Andrew Hunt

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Education

Texas A&M University, MS in Computer Engineering — Fall 2023 – May 2025

- GPA: 3.61
- **Coursework:** Advanced Hardware Design Verification, Advanced Computer Architecture, Microprogrammed Control of Digital Systems, Computer Arithmetic Unit Design, Field Programmable Gate Arrays, Analysis of Algorithms

Texas A&M University, BS in Electrical Engineering — Fall 2020 – May 2023

- GPA: 3.59 Cum laude
- **Coursework:** Computer Architecture, Microprocessor System Design, Digital IC Design, Computational Data Science, Advanced Digital Design

Lonestar College, AS in Electrical Engineering — December 2019

- Magna Cum Laude

Experience

Network Technician, United States Air Force – San Antonio, TX — Jan 2010 – Jan 2016

- Installed and maintained network appliances and VOIP technology for a campus area network supporting over 5000 users
- Investigated network issues and provided solutions while keeping customer downtime to a minimum
- Trained and mentored junior technicians on network troubleshooting and repair
- Automated process for generating IT ticket reports, reducing time required from eight hours each week to two
- Presented weekly reports to IT leadership on the status of IT service tickets

Computer Technician, Neobox Computers – The Woodlands, TX — Jan 2007 – Jun 2009

- Investigated and solved computer hardware and malware issues to meet customer needs in store, on location, and over the phone
- Built and configured new computers fitting the usecases of the customer
- Interfaced with vendors and manufacturers to resolve customers' warranty issues
- Analyzed and overcame issues resulting from new forms of malware that were resistant to existing software

Projects

L-TAGE Branch Predictor — 2025

- Developed an L-TAGE branch predictor with variable length history and number of tables
- Tools Used: C++, Python, Bash

Pipelined RISC CPU — 2024

- Implemented a five stage pipelined RISC CPU with basic branch prediction and hazard detection
- Tools Used: Verilog

SD Card interface — 2024

- Developed an SD Card interface on an FPGA with an SPI driver and a variable length CRC systolic array
- Tools Used: Verilog

Technologies

Skills: Design Verification, Digital Design, Computer Architecture, VLSI Design, RTL Design
Languages: Verilog, SystemVerilog, UVM, Python, C, C++, Java, Bash
Software: Xilinx, Cadence, Synopsys, Linux, Git
Training: Cadence SystemVerilog for Design and Verification, Cadence SystemVerilog Accelerated Verification with UVM, Cadence VIP Building Blocks and Usage